Published Attached

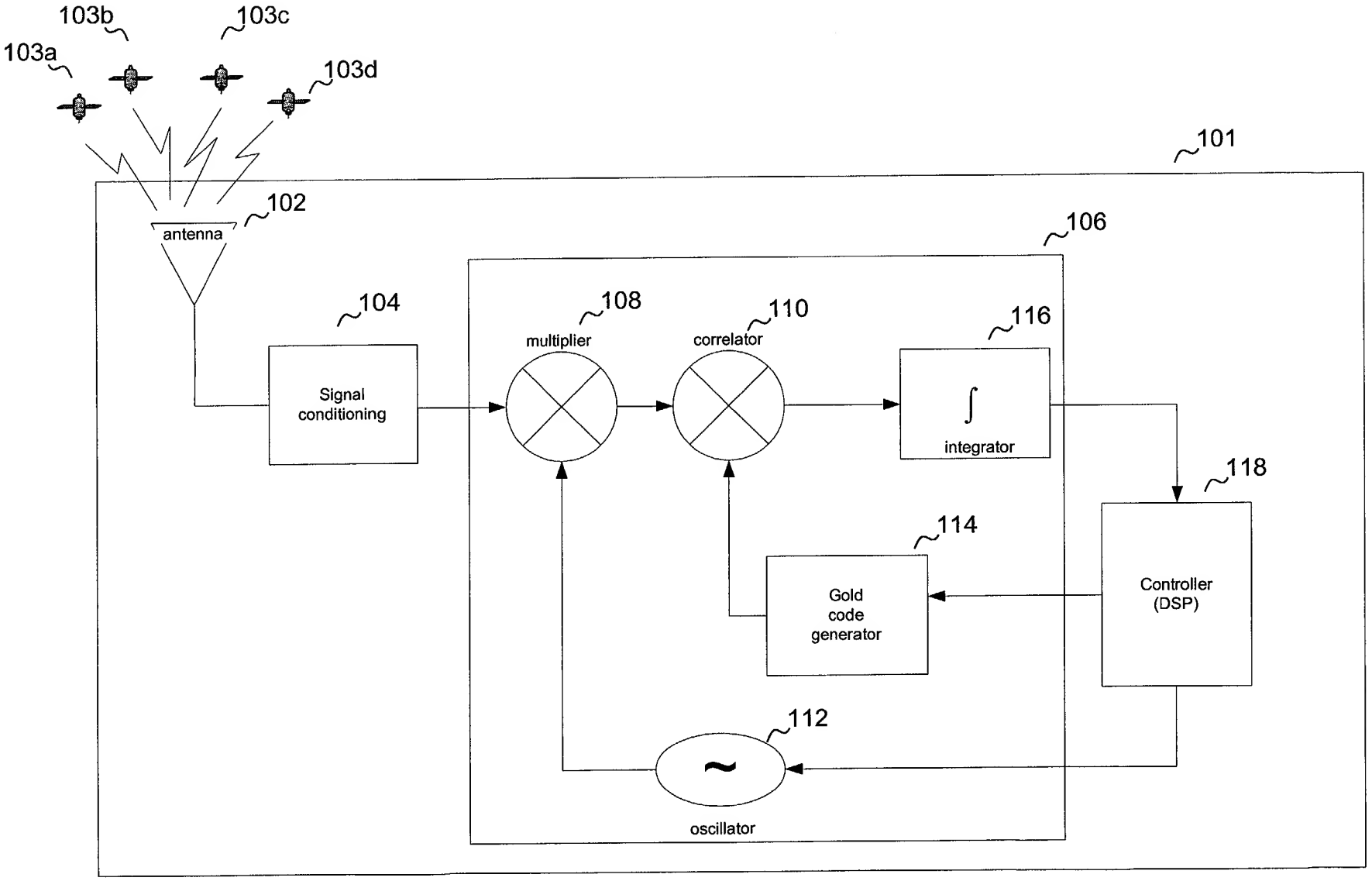

FIGURE 1
(PRIOR ART)

Loaded Instead

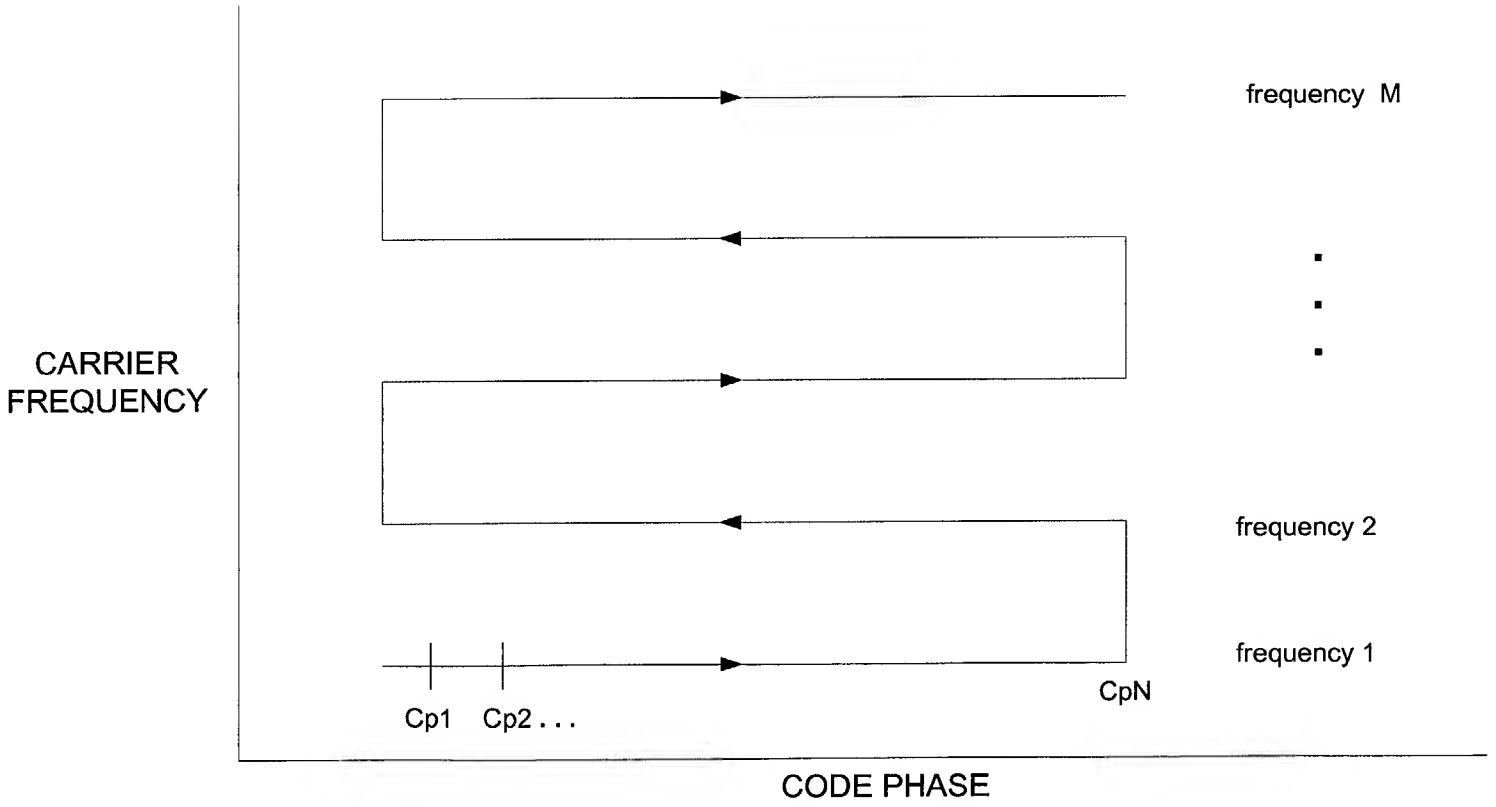

FIGURE 2
(PRIOR ART)

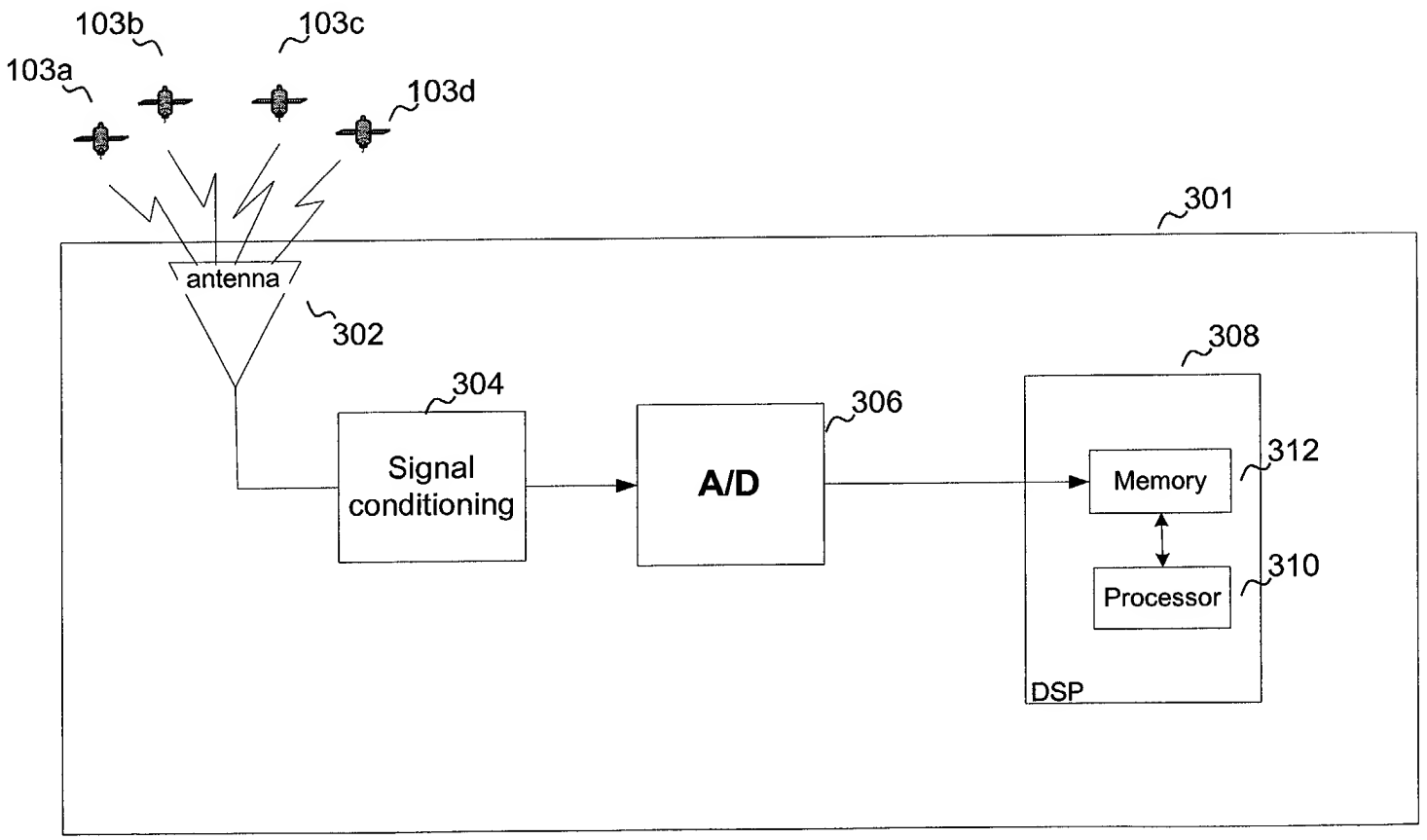
103b
103c
103a
103d
301
antenna
302
304
308
306
Signal conditioning
A/D
Memory
312
310
Processor
DSP

FIGURE 3

Docket #13436.0

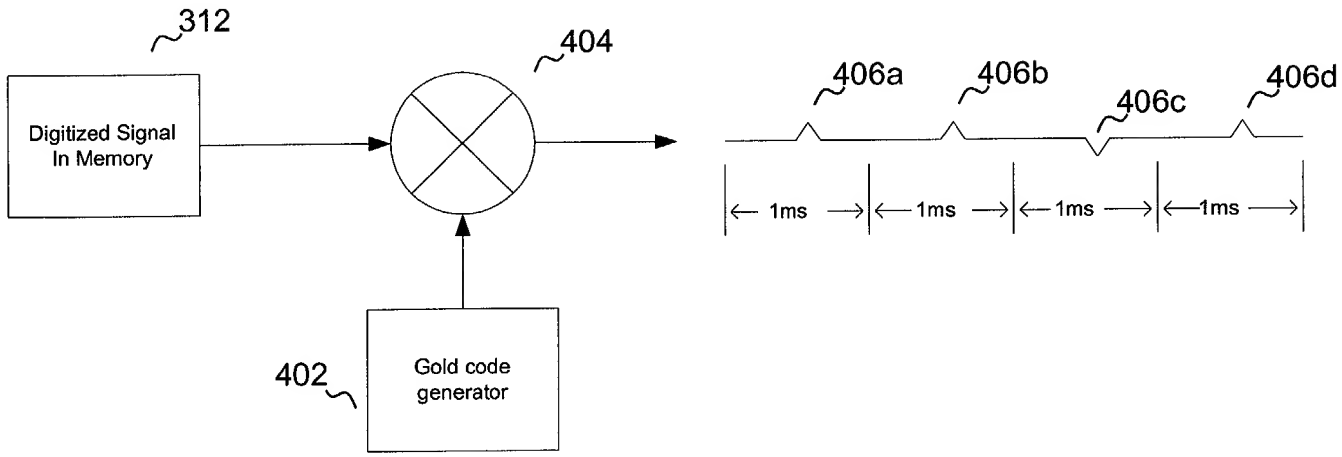

FIGURE 4

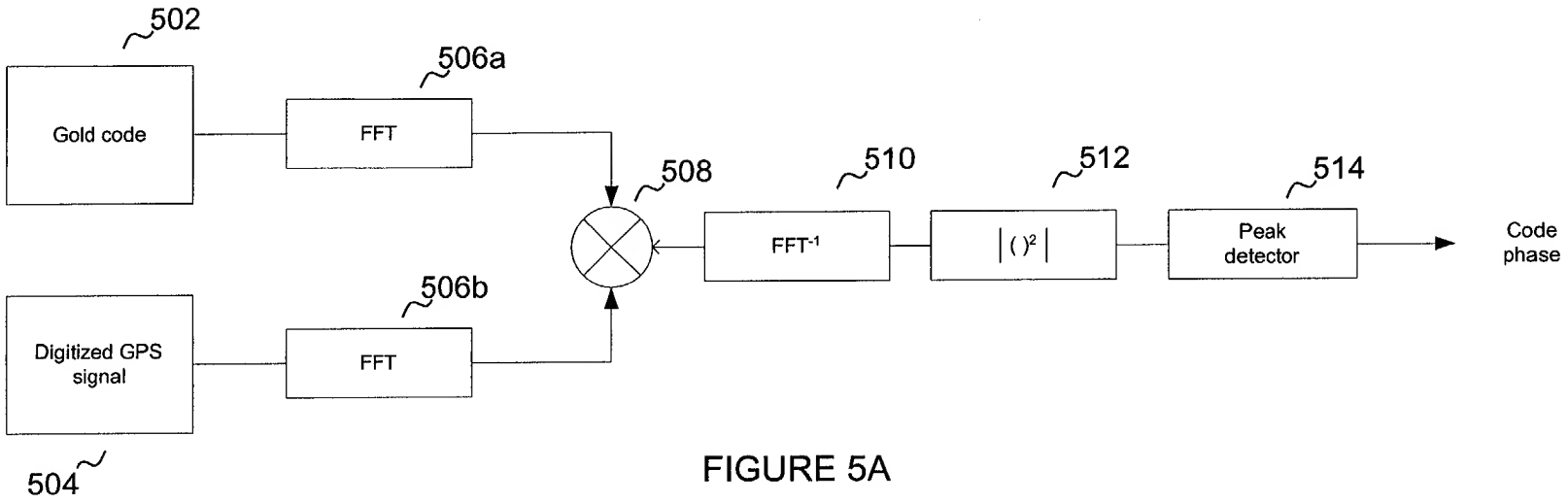

FIGURE 5A

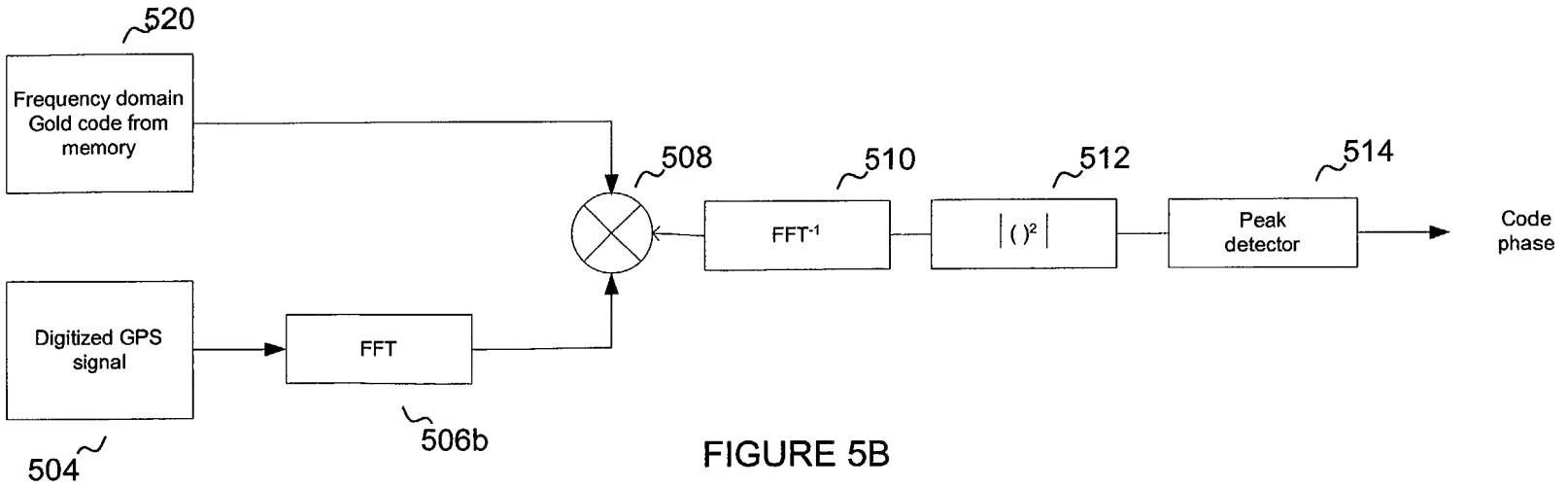

FIGURE 5B

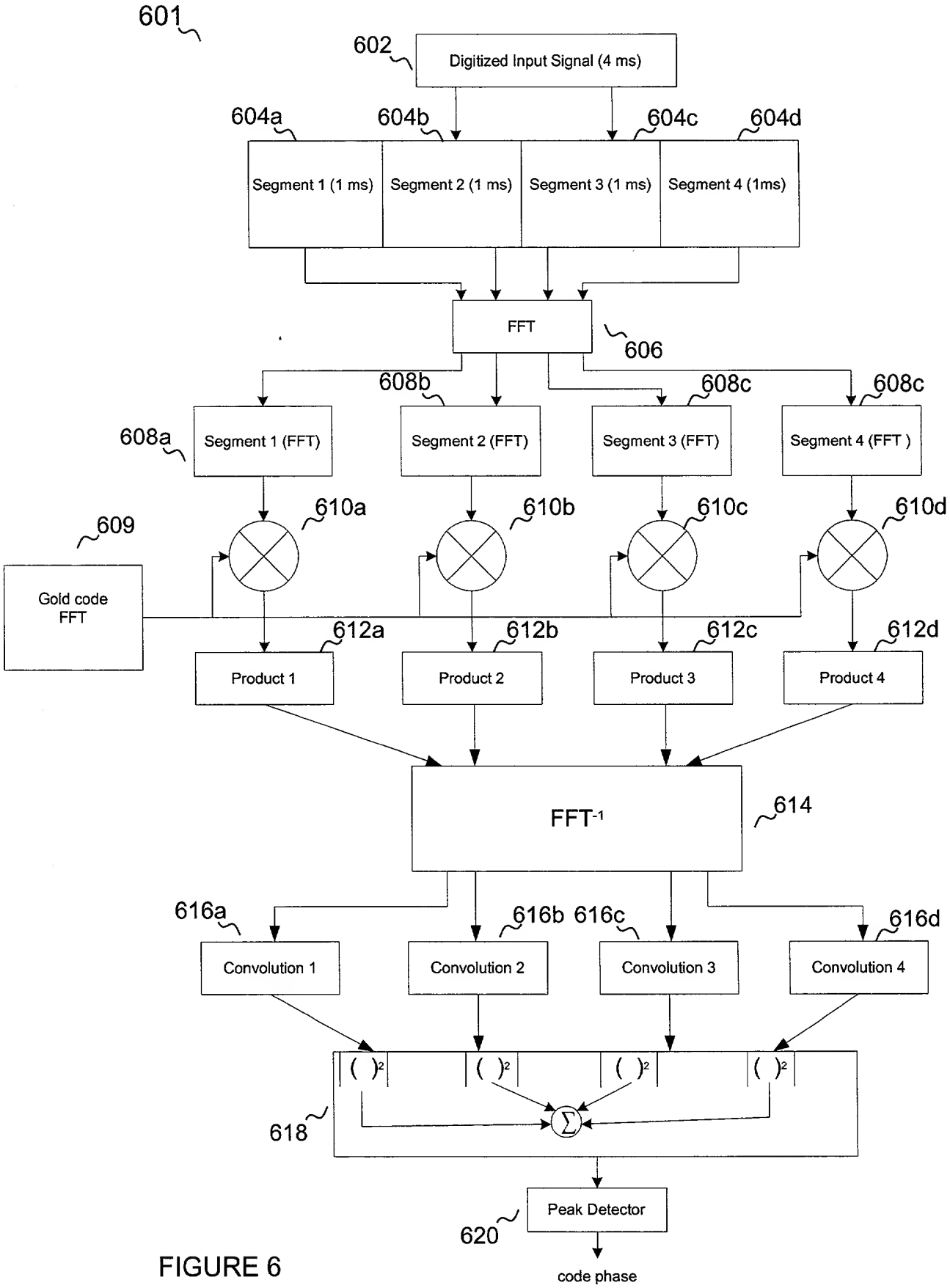
601
602
Digitized Input Signal (4 ms)
604a
604b
604c
604d
Segment 1 (1 ms)
Segment 2 (1 ms)
Segment 3 (1 ms)
Segment 4 (1ms)
FFT
606
608a
608b
608c
608c
Segment 1 (FFT)
Segment 2 (FFT)
Segment 3 (FFT)
Segment 4 (FFT)
609
610a
610b
610c
610d
Gold code FFT
612a
612b
612c
612d
Product 1
Product 2
Product 3
Product 4
FFT-1
614
616a
616b
616c
616d
Convolution 1
Convolution 2
Convolution 3
Convolution 4
( )2
( )2
( )2
( )2
Σ
618
Peak Detector
620
code phase

FIGURE 6

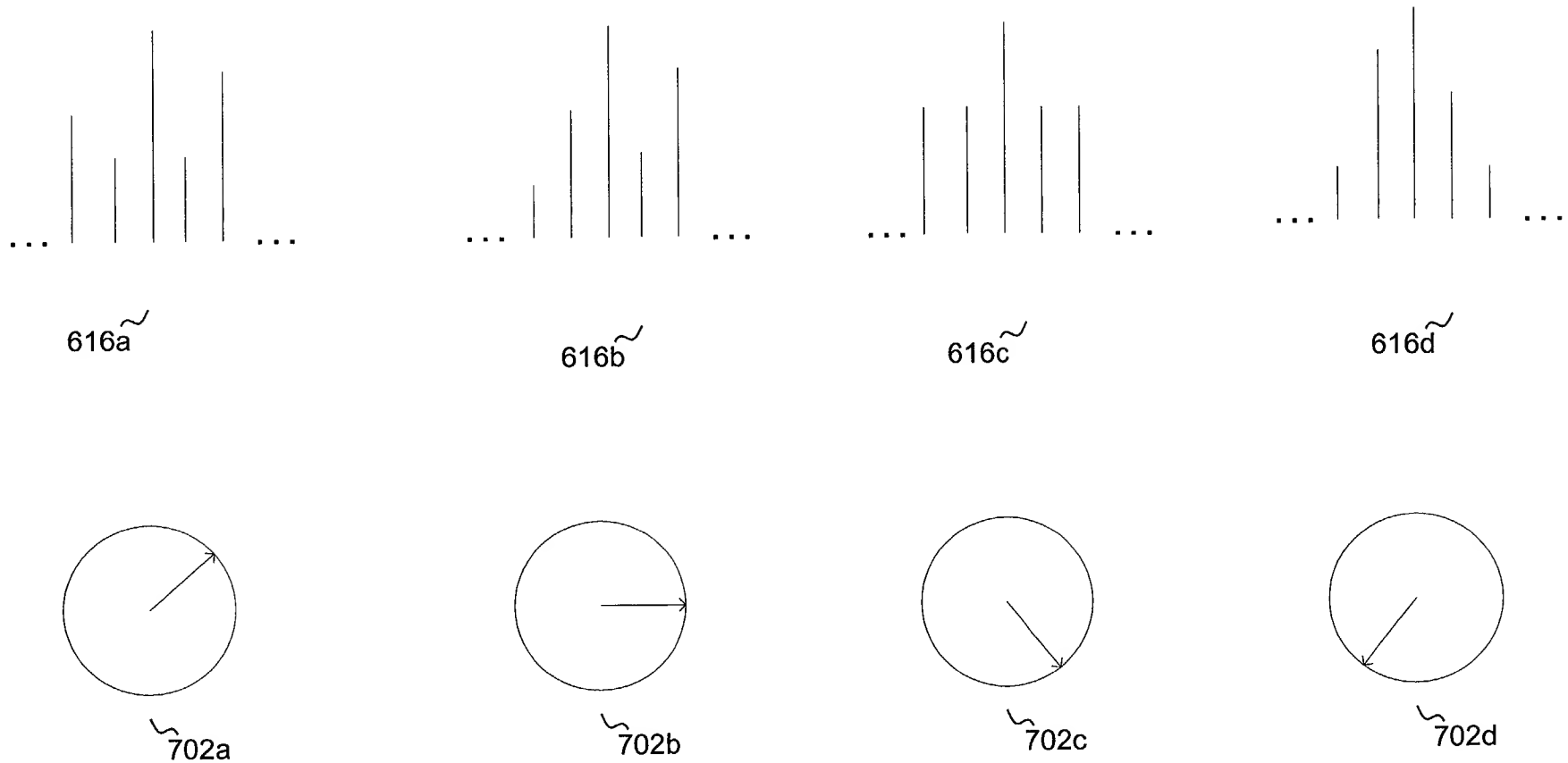

FIGURE 7

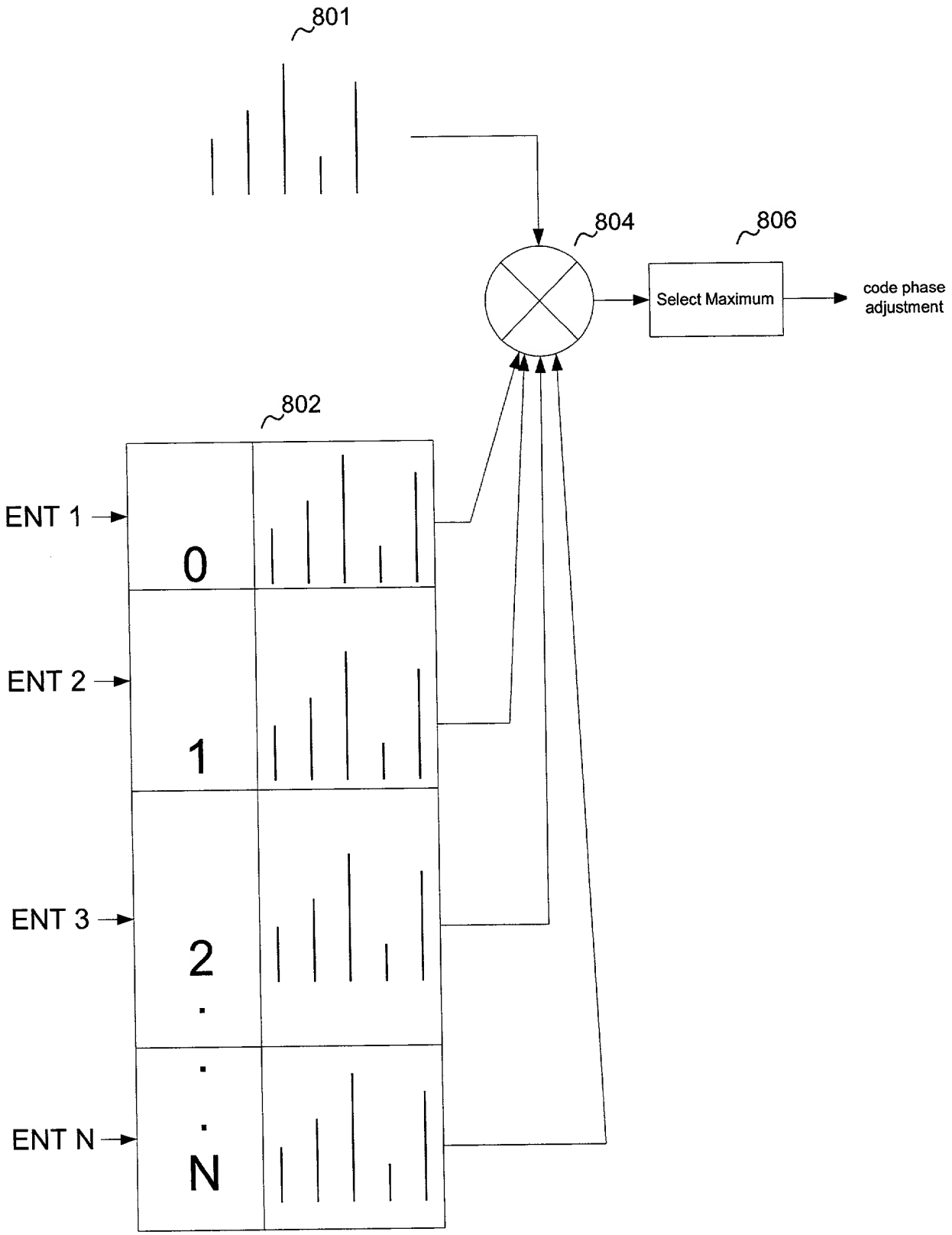
801
804
806
Select Maximum
code phase adjustment
802
ENT 1
0
ENT 2
1
ENT 3
2
ENT N
N

FIGURE 8